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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,286	11/19/2003	Gabriel L. Romero	LSI.87US01 (03-0760)	1213

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EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 07/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,286	ROMERO ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER 6/13/2006
GROUP 2100
AU2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 have been examined.

Acknowledgment of papers filed: oath, specification, drawings and IDS on 19 November 2003. The papers filed have been placed on record.

Claim Objections

2. Claim 2 is objected to because the limitation "having first and second expander cores" renders the claim unclear. It is unclear whether there can be multiple first expander cores or multiple second expander cores. Examiner suggests the limitation read "having a first expander core and a second expander core". Examiner also suggests the limitation "said first and second expander cores" (occurring twice) read "said first expander core and said second expander core".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by IEEE (IEEE Standard Test Access Port and Boundary-Scan Architecture).

5. Regarding claim 1, IEEE discloses a process for controlling a multiple core expander (see page 14, fig. 4-1) comprising: using a test port (Path between TDI and TDO)

Note that the definition of "port" according to The Free On-line Dictionary of Computing, © 1993-2005 is "A logical channel or channel endpoint in a communications system." According to this definition, the connection path through all components from TDI and TDO can be considered a port.

Of said multiple core expander to send operational codes (Instructions; see page 36, section 8) to said multiple core expander to put all but one core of said multiple core expander in bypass mode (Bypass instruction; see pages 38-39, section 8.4); serially reading data from (Sample instruction; see pages 41-43; section 8.6), and serially writing data to (Preload instruction; see pages 43-45; section 8.7), at least one internal register (boundary scan registers) of said one core through said test port.

6. Regarding claim 2, IEEE discloses a method of controlling the operation of a dual expander having first and second expander cores (first two components; see page 14, fig. 4-1) by reading and writing control bits through a single test port (see above regarding claim 1) in said dual expander comprising: placing one of said first and second expander cores in bypass mode (see above regarding claim 1); transmitting a serial data stream of said control bits through said test port to a shift register (Shift

Register Stage) to generate a control byte; parallel shifting said control byte from said shift register to a control register (Parallel Output; see pages 34-36; section 7.2; Table 7-1) in one of said first and second expander cores that is not in bypass mode; providing dummy bits as needed in said serial data stream to correctly form said control byte (see page 39; section 8.4.2).

Note that all devices in bypass mode only require one bit (dummy bit) in the serial stream and the only real data is for the device not in bypass mode. Further note that the term "as needed" renders the use of dummy bits unnecessary because if they are not used, they are inherently not needed.

7. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by CYGNAL (Programming FLASH through the JTAG Interface).

8. Regarding claim 3, CYGNAL discloses a process for performing a register write operation (Indirect Write, see page 8) in a first expander core (isolated device) of a dual expander comprising: serially shifting operational code bits (BYPASS instruction for all other devices in the chain) into a test port (TDI), said operational code bits including instructions to place a second expander core, in said dual expander, in bypass mode (JTAG_IR_Scan function, see pages 38-40); generating an operational byte (the BYPASS opcode)

Note that typically a byte consists of 8 bits, but can also be used to describe the smallest addressable memory segment in a computer. In this case, a single instruction can be considered a byte.

From said operational code bits; placing said second expander core in bypass mode in response to said operational byte (see page 39, last 4 lines); shifting a dummy bit into said test port (see page 40, for loop for filling the BYPASS Register of the devices before the isolated device with zeros.); serially shifting control bits (Write Data yyyy, see page 9, fig. 10; page 39), address bits (xxx; see page 9, fig. 10; page 39) and write command bits (11; see page 8, IndOpCode Decoding; page 41 regarding appending 'WRITE' opcode to data) into said test port; generating a control byte from said control bits and an address byte from said address bits (see page 6 regarding loading data and instruction registers after the data is serially shifted to them);

Note that as stated above, the control bits and address bits are fed into the Shift_IR and Shift_DR.

Writing said control byte to a register in said first expander core at an address indicated by said address byte (see page 8, Indirect Write section, first 2 lines).

9. Claim 4 recites equivalent limitations as claim 3 and is therefore rejected under the same grounds.

*Note that the names "first expander" and "second expander" do not limit the invention, but merely state different labels for an element. There*fore, both claims are anticipated by communication of any device of a JTAG chain. Further note that while

the limitations are claimed in different order in claims 3 and 4, there is no limitation which places these elements of the process in a specific chronological order.

10. Claims 5 and 6 recite equivalent limitations as claims 3 and 4 but claim the method of reading a register instead of writing it. These claims are anticipated by the Indirect Read instruction (see page 8). The two operations are equivalent except for the following:

Operation code is "10" instead of "11" (see page 18).

The data is read serially read from the register in the isolated expander core at the address indicated by the address byte (as claimed, see page 8, first 2 lines of Indirect Read section; pages 49-50).

Note that the read and write operations are executed using the same function (JTAG_DR_Scan).

11. Claims 1 and 2 recite similar and less broad limitations as claims 3-6 with the exception of the following limitations:

"to put all but one core of said multiple core expander in bypass mode", which is disclosed by CYGNAL (see JTAG_IR_Scan; page 38);

and "parallel shifting said control byte from said shift register to a control register", which is disclosed by CYGNAL (Update-DR; see page 5, fig. 6).

Conclusion

12. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 6/21/06

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